



11-30-01

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No. VAO-004.01

First Inventor Downey, Daniel F.

Title Athermal Annealing With Rapid Thermal Annealing System and Method

Express Mail Label No. EL-719917836 US



APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. Applicant claims small entity status.
See 37 CFR 1.27.
3. Specification [Total Pages 20]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to sequence listing, a table, or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. Drawing(s) (35 U.S.C.113) [Total Sheets 7]
5. Oath or Declaration [Total Pages 27]
 - a. Newly executed (original or copy)
 - b. Copy from a prior application (37 CFR 1.63 (d))
(for a continuation/divisional with Box 18 completed)
 - i. **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. Application Data Sheet. See 37 CFR 1.76

ADDRESS TO: Commissioner for Patents
Box Patent Application
Washington, DC 20231

7. CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. CD-ROM or CD-R (2 copies); or
 - ii. paper
 - c. Statements verifying identity of above copies

ACCOMPANYING APPLICATIONS PARTS

9. Assignment Papers (cover sheet & document(s))
10. 37 C.F.R. §3.73(b) Statement Power of Attorney (when there is an assignee)
11. English Translation Document (if applicable)
12. Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS Citations
13. Preliminary Amendment
14. Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
15. Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. Other: Request for Non-Publication

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

Continuation Divisional Continuation-in-part (CIP) of prior application No: _____ / _____
Prior application information: Examiner _____ Group / Art Unit: _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

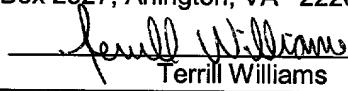
<input checked="" type="checkbox"/> Customer Number or Bar Code Label		25181	<input type="checkbox"/> Correspondence address below	
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Name (Print/Type)	Kevin A. Oliver	Registration No. (Attorney/Agent)	42,049
Signature			Date 11/28/01

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Terrill Williams

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$ 780.00)

Complete if Known	
Application Number	
Filing Date	November 28, 2001
First Named Inventor	Downey, Daniel F.
Examiner Name	
Group / Art Unit	
Attorney Docket No.	VRO-004.01

METHOD OF PAYMENT (check one)

1. The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number 06-1448

Deposit Account Name

Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

Applicant claims small entity status. See 37 CFR 1.27

2. Payment Enclosed:

Check Credit card Money Order Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee (\$)	Small Entity Fee Code	Fee Description	Fee Paid
101	740	201	370	Utility filing fee
106	330	206	165	Design filing fee
107	510	207	255	Plant filing fee
108	740	208	370	Reissue filing fee
114	160	214	80	Provisional filing fee

SUBTOTAL (1)

(\$ 740.00)

2. EXTRA CLAIM FEES

Total Claims	17	20	=	0	X	Fee from below	=	0	Fee Paid
Independent Claims			-	**	=	0	X	0	
Multiple Dependent					X			0	

Large Fee Code	Entity Fee (\$)	Small Entity Fee Code	Fee Description
103	18	203	9 Claims in excess of 20
102	84	202	42 Independent claims in excess of 3
104	280	204	140 Multiple dependent claim, if not paid
109	84	209	42 ** Reissue independent claims over original patent
110	18	210	9 ** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

(\$!Undefined
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TEXT130)

FEE CALCULATION (continued)

3. ADDITIONAL FEES	Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105	130	205	65 Surcharge - late filing fee or oath	
127	50	227	25 Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130 Non-English specification	
147	2,520	147	2,520 For filing a request for reexamination	
112	920*	112	920* Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840* Requesting publication of SIR after Examiner action	
115	110	215	55 Extension for reply within first month	
116	400	216	200 Extension for reply within second month	
117	920	217	460 Extension for reply within third month	
118	1,440	218	720 Extension for reply within fourth month	
128	1,960	228	980 Extension for reply within fifth month	
119	320	219	160 Notice of Appeal	
120	320	220	160 Filing a brief in support of an appeal	
121	280	221	140 Request for oral hearing	
138	1,510	138	1,510 Petition to institute a public use proceeding	
140	110	240	55 Petition to revive – unavoidable	
141	1,280	241	640 Petition to revive – unintentional	
142	1,280	242	640 Utility issue fee (or reissue)	
143	460	243	230 Design issue fee	
144	620	244	310 Plant issue fee	
122	130	122	130 Petitions to the Commissioner	
123	50	123	50 Processing fee under 37 CFR 1.17 (q)	
126	180	126	180 Submission of Information Disclosure Stmt	
581	40	581	40 Recording each patent assignment per property (times number of properties)	40.00
146	740	246	370 Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370 For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370 Request for Continued Examination (RCE)	
169	900	169	900 Request for expedited examination of a design application	
Other fee (specify) _____				

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$ 40.00)

**or number previously paid, if greater; For Reissues, see above

SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	Kevin A. Oliver	Registration No. Attorney/Agent)	42,049
Signature		Telephone	617-832-1241

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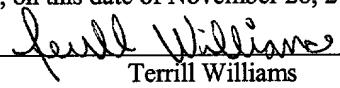
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Terrill Williams

**REQUEST AND CERTIFICATION
UNDER
35 U.S.C. 122(b)(2)(B)(i)**

First Named Inventor	Downey, Daniel F.
Title	ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD
Atty Docket Number	VRO-004.01

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

11/28/2001
Date

Kevin A. Oliver
Signature

Kevin A. Oliver 42,049

Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

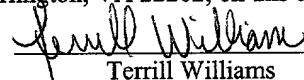
If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

EXPRESS

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Terrill Williams

01595647463 2001-11-28 01:45

NOTICE OF FEE DUE

DATE: 12-3-01

TO: U1

FROM: Office of Initial Patent Examination

SUBJECT: Fee Due \$ 740

APPLICATION NUMBER: _____

A fee is due for the attached document submitted to the U. S. Patent and Trademark Office for the following reason. Please check the application for the appropriate authorization to charge a deposit account. If an authorization is present, please charge the appropriate fee. If an authorization is not present, notify the applicant of the fee deficiency.

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The correct fee code: _____ amount \$ _____

The suspended fee code: 197 amount - \$

Fee Due amount = \$ _____

If you have any questions, please contact Cynthia Streater at 703-306-5430 or Eleanor Kurtz at 703-308-3642.

Terminal Operator _____

APPLICATION
FOR
UNITED STATES LETTERS PATENT
ENTITLED

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

TO WHOM IT MAY CONCERN:

BE IT KNOWN THAT (1) DANIEL F. DOWNEY and (2) EDWIN A. AREVALO of (1) 8 Ryan Road Gloucester, MA 01930, and (2) 34 Miriam Road, Waltham, MA 02451, invented certain new and useful improvements entitled as set forth above of which the following is a specification:

PATENT GROUP
FOLEY, HOAG & ELIOT LLP
ONE POST OFFICE SQUARE
BOSTON, MA 02109-2170
TEL: 617-832-1000
FAX: 617-832-7000

3 ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD
4

5 BACKGROUND
6

7 (1) Field
8

9 The disclosed methods and systems relate generally to
10 annealing processes, and more particularly to athermal annealing.
11

12 (2) Description of Relevant Art
13

14 Conventional ion implantation systems include ionizing a
15 dopant material such as boron, accelerating the ions to form an
16 ion beam having a given energy level, and directing the ion beam
17 energy at a semiconductor surface or wafer to introduce the
18 dopant material to the semiconductor and alter the conductivity
19 properties of the semiconductor. Once the ions are embedded into
20 the crystalline lattice of the semiconductor, the ions can be
21 activated using a process known as rapid thermal annealing (RTA)
22 or rapid thermal process (RTP). During RTA, the semiconductor
23 can be introduced to a furnace to heat the semiconductor at a
24 prescribed temperature and for a prescribed time. RTA can also
cure defects in the crystalline structure that can be caused by
the ion implantation.

The processes of ion implantation and RTP contribute to the
depth of the implanted region, known as the junction depth.

1 Those of ordinary skill in the art recognize that the junction
2 depth from ion implantation is based on the energy of the ions
3 implanted into the semiconductor. Accordingly, shallow implanted
4 regions can be formed using low-energy ion beams. Unfortunately,
5 traditional methods of RTA include raising the temperature of the
6 silicon to ranges nearing 1100-1200 degrees Celsius, which can
7 approach the melting temperature of the silicon. Accordingly,
8 RTA can further increase the implanted junction depth as high
9 temperatures of the RTA process cause further diffusion of the
10 implanted region.

11 The increase in junction depth can be particularly
12 troublesome when considered with respect to a continuing and
13 expanding demand for smaller devices, and hence shallower
14 junction depths. It is anticipated that the present methods and
15 systems that combine ion implantation solely with traditional RTA
16 may not satisfy the demand for shallower junctions.

17

18 SUMMARY

19 The disclosed methods and systems include features for
20 annealing a semiconductor structure that include subjecting the
21 semiconductor structure to an oscillating magnetic field and
22 applying a low temperature rapid thermal annealing (LTRTA)
23 process to the semiconductor structure. The electromagnetic
24 field can be a time-varying electromagnetic field that can be

1 provided by, for example, a signal having a frequency in the
2 microwave or the radio frequency (RF) bands.

3 In one embodiment, the LTRTA can include exposing the
4 semiconductor to a temperature less than approximately 800
5 degrees Celsius, while in another embodiment, the temperature can
6 be greater than approximately 500 degrees Celsius, and less than
7 approximately 800 degrees Celsius. The RTA can be performed in a
8 furnace or another annealing device.

9 For the disclosed methods and systems, the LTRTA can be
10 performed either before or after the application of
11 electromagnetic field or energy.

12 The methods and systems can accordingly be implemented with
13 and/or applied to ion implantation systems where dopant material
14 ions can be implanted into a semiconductor structure or wafer.
15 The semiconductor wafer can include silicon or Gallium Arsenide,
16 for example. The dopant can be any one of an n-type dopant and a
17 p-type dopant.

18 Other objects and advantages will become apparent
19 hereinafter in view of the specification and drawings.

20

21 BRIEF DESCRIPTION OF THE DRAWINGS

22 FIG. 1 is one embodiment of a system and method for
23 performing Electromagnetic Induction Heating (EMIH) annealing
24 using microwave frequencies;

1 FIG. 2A is a TM011 magnetic field pattern;

2 FIG. 2B is a TM111 magnetic field pattern;

3 FIG. 3 is one embodiment of a radio frequency system and
4 method for performing EMIH annealing;

5 FIG. 4 displays a relationship between power absorption and
6 conductivity;

7 FIG. 5 displays a relationship between conductivity and
8 temperature for various dopant levels;

9 FIG. 6 includes a SEMATECH barrier curve for evaluating
10 improvements in anneal and doping technology; and,

11 FIG. 7 provides a SIMS profile for as-implanted and
12 microwave spike annealed plasma doped (PLAD) samples.

13
14 DESCRIPTION

15 To provide an overall understanding, certain illustrative
16 embodiments will now be described; however, it will be understood
17 by one of ordinary skill in the art that the systems and methods
18 described herein can be adapted and modified to provide systems
19 and methods for other suitable applications and that other
20 additions and modifications can be made without departing from
21 the scope of the systems and methods described herein.

22 Unless otherwise specified, the illustrated embodiments can
23 be understood as providing exemplary features of varying detail
24 of certain embodiments, and therefore features, components,

1 modules, and/or aspects of the illustrations can be otherwise
2 combined, separated, interchanged, and/or rearranged without
3 departing from the disclosed systems or methods.

4 During ion implantation, the implanted regions can be
5 damaged when the accelerated, energized dopant ions collide with
6 the host or silicon surface, displacing silicon atoms from their
7 original lattice sites. Although the dopant ions can be in high-
8 energy non-equilibrium positions in the silicon lattice, the
9 dopant ions are not electrically active. A rapid thermal
10 annealing (RTA) process can provide energy to the silicon and
11 dopant ions to allow movement of the ions to equilibrium
12 positions, thereby also repairing the implantation damage by
13 restoring crystallographic order. Unfortunately, the RTA process
14 that exposes the semiconductor surface to high temperatures in
15 the range of 1000-1200 degrees Celsius, often also causes dopant
16 redistribution or diffusion. RTA for certain implant doses can
17 increase junction depths to be significantly deeper than, for
18 example, the as-implanted range.

19 For example, with regard to transistor devices, the
20 consequences of a continued demand for small devices can be
21 anticipated to include a limiting of lateral diffusion under the
22 gate and a maintenance of high concentration of dopant material
23 in a shallow source/drain extension region. Accordingly, the
24 disclosed methods and systems include a combination of athermal

1 annealing and rapid thermal annealing (RTA) to obtain a very
2 shallow junction with a device having a low sheet resistance.
3 The methods and systems accordingly utilize electromagnetic
4 fields to induce current flow through a silicon wafer and cause
5 ohmic collisions between high energy electrons and the silicon
6 lattice structure to provide rapid heating of the silicon from
7 within the structure, as opposed to RTA that applies high
8 temperatures to the structure surface. The athermal heating of
9 the silicon, referred to herein as Electromagnetic Induction
10 Heating (EMIH), provides energy to activate the dopant that can
11 provide greater activation than a method or system using RTA
12 (also referred to and known as RTP). Low temperature RTA
13 (LTRTA), understood herein to be temperatures less than
14 approximately 800 degrees Celsius, but for the illustrated
15 embodiments, preferably between approximately 500 degrees Celsius
16 and approximately 800 degrees Celsius, can also be performed
17 before and/or after the EMIH to further repair the silicon
18 structure and minimize diffusion. LTRTA can be performed at a
19 temperature, and for a time period, that can be significantly
20 less than generally associated with processes that only use RTA
21 annealing for dopant activation and crystallographic defect
22 curing. Those of ordinary skill in the art recognize that merely
23 using LTRTA can fail to activate the dopant and hence can result
24 in a large sheet resistance. Accordingly, by combining the

1 athermal annealing to provide dopant activation and the LTRTA
2 (approximately 500-800 degrees Celsius) RTA to cure the
3 structural defects, the dopant material can be activated, the
4 lattice structure can be repaired, and differences between the
5 as-implanted junction depth and the post-annealing junction depth
6 can be minimized when compared to methods that use only RTA.

7 EMIH can be understood as a unique application of Faraday's
8 and Ampere's laws. As a silicon wafer is exposed to oscillating
9 magnetic fields, electrons are induced to flow within the wafer.

10 As the electrons collide with the lattice, they release energy
11 that heats the silicon wafer. This athermal, internal heating
12 via EMIH can be compared to, for example, RTA that generally
13 exposes the wafer to a furnace at a prescribed temperature and
14 causes the silicon to be heated from the outside surface in,
15 thereby raising a possibility of silicon melt.

16 Those with ordinary skill in the art recognize that for
17 highly conducting materials such as copper, induced currents re-
18 induce a magnetic field that partially or completely interferes
19 with the incident electromagnetic field. Alternately, insulating
20 materials such as quartz lack free carriers and hence preclude
21 any flow of current, thereby allowing the incident field to
22 penetrate the material. Semiconductors such as silicon can have
23 properties of conductors and insulators, and thus can have a

1 potential for significant electromagnetic field penetration that
2 can induce substantial currents throughout the wafer volume.

3 In the disclosed methods and systems, electromagnetic fields
4 can be induced by subjecting the silicon sample to
5 electromagnetic energy having frequencies in the radio frequency
6 (RF) and microwave ranges, although those with ordinary skill in
7 the art will recognize that the methods and systems are not
8 limited to these frequency ranges, and other methods of inducing
9 electromagnetic energy can be used. The rapid, internal ohmic
10 heating of the wafers caused by the induced currents in the
11 silicon wafer can cause dopant activation that can be more
12 effective than the activation that can be caused by the surface
13 heating provided by RTA.

14 Referring now to FIG. 1, there is one embodiment of a
15 microwave system that includes a resonant cavity having a radius
16 of seventeen centimeters, and a height that can be adjusted
17 between fifteen and forty-five centimeters for tuning to specific
18 microwave modes. A magnetron source can provide a maximum three
19 thousand watts of power at 2.45GHz. One of ordinary skill in the
20 art will recognize that various modes can be provided by a system
21 according to FIG. 1, including but not limited to the well-known
22 TM011 and TM111 modes. FIGS. 2A and 2B provide magnetic field
23 patterns in the FIG. 1 microwave cavity for the TM011 and TM111
24 modes, respectively.

1 Referring to FIG. 3, there is a RF embodiment of the
2 disclosed methods and systems that utilizes an exciting RF
3 magnetic flux with a spiral copper antenna. A power supply
4 matched through an L-type matching network can provide up to one-
5 thousand Watts at a fixed 13.56MHz frequency. In the FIG. 3
6 system, a silicon wafer can be positioned on a ceramic chuck two-
7 and-a-half centimeters below the coil windings in an extreme near
8 field of the antenna. In the illustrated system, the ceramic
9 chuck can be heated to one-hundred fifty degrees Celsius.

10 Those with ordinary skill in the art will recognize that the
11 exemplary electromagnetic induction systems of FIGs. 1 and 3 are
12 merely illustrative and the implementation thereof is not limited
13 to the embodiments or characteristics provided herein.

14 Furthermore, although FIGs. 2A and 2B provide two magnetic field
15 patterns, such patterns are provided for illustration and not
16 limitation. Accordingly, other systems that utilize alternate
17 methods, frequencies, apparatus, magnetic field patterns, fewer
18 or additional components or alternatives, etc., can be used
19 without departing from the scope of the methods and systems
20 disclosed herein.

21 For the illustrated systems of FIGs. 1 and 3, temperature
22 measurements can be provided by collecting radiated light using
23 an optical pyrometer or light pipe. The collected radiated light
24 can be analyzed by, for example, a Luxtron model analyzer that

1 matches the collected light intensities to a black body radiation
2 spectrum to produce a temperature of the silicon wafer. In some
3 embodiments, the spectrum may be modified or scaled to provide an
4 accurate temperature measurement based on the emissivity of
5 silicon.

6 The EMIH methods and systems can allow a prediction of a
7 magnitude of the induced currents, and hence, the temperature.
8 As provided previously herein, a solution of Faraday's and
9 Ampere's laws can provide a description of the induced current
10 density and the power absorbed, where:

$$11 P_{ABS} = \frac{\pi a^2 t_w^3 / (\delta^4 \sigma)}{1 + (t_w / \delta)^4} H_0^2 \quad , \quad \delta = \sqrt{2 / \omega \mu \sigma} \quad (1)$$

12 where δ is skin depth, ω is frequency, μ is permeability, σ is
13 conductivity, t_w is thickness, "a" is radius, and H_0 is the
14 incident magnetic field. FIG. 4 provides a plot of power
15 absorption based on conductivity according to Equation 1. As
16 FIG. 4 and Equation 1 indicate, the absorbed power increases with
17 conductivity, σ , until a peak absorption is reached. Thereafter,
18 the absorbed power decreases at the same rate of the increase and
19 asymptotes to zero.

20 The relationship between temperature and conductivity can be
21 instrumental to understanding the FIG. 4 relationship between
22 power absorption and conductivity. FIG. 5 provides the
23 relationship between conductivity and temperature for a variety
24 of substrate doping levels. It is well-known that although

1 conductivity can be expressed as a product of mobility and
2 carrier density, mobility decreases with temperature due to an
3 increased collision frequency that impedes carrier flow, while
4 carrier density increases with temperature as the increased
5 thermal energy moves carriers from the valence band to the
6 conduction band. Accordingly, as FIG. 5 indicates, conductivity
7 can decrease until the temperature exceeds approximately one-
8 hundred degrees Celsius, during which time collisions impede
9 carrier mobility. As the temperature further increases, the
10 increase in intrinsic carriers can exceed the loss in mobility to
11 allow the conductivity to monotonically increase with
12 temperature. The largest conductivity illustrated in FIG. 5
13 relates to the peak power absorption level in FIG. 4, and
14 accordingly, when viewing FIGs. 4 and 5 together as a function of
15 increasing temperature, it can be seen that for the smaller
16 illustrated levels of doping, as temperature increases to
17 approximately one-hundred degrees Celsius, conductivity (FIG. 5)
18 decreases and hence power absorption (FIG. 4) is also decreasing,
19 thereby preventing the wafer temperature from increasing. This
20 can otherwise be known as an absorption valley. As the wafer
21 temperature increases beyond this temperature (FIG. 5), however,
22 conductivity increases with temperature, thereby also causing an
23 increase in power absorption (FIG. 4) that can cause a rapid
24 increase in temperature. At approximately five-hundred degrees

1 Celsius, the intrinsic carrier concentration can greatly exceed
2 the doping such that the conductivity, and hence heating, becomes
3 independent of the substrate doping, and silicon wafers of
4 varying dopant dosages can heat with identical characteristics.

5 Based on FIG. 4 and 5, and the inference that higher
6 frequency fields (e.g., microwave) can heat more efficiently than
7 lower frequency fields (e.g., RF), in some embodiments, it can be
8 necessary to pre-heat the silicon wafer to a temperature above
9 the absorption valley. In some embodiments, for given power
10 levels, the same wafer temperature can be achieved irrespective
11 of whether one or more wafers are present. Accordingly, batch
12 processing can be equally as effective.

13 In one embodiment of the methods and systems, B^+ and BF_2^+
14 ions, at a dose of $10^{15}/cm^3$, were implanted into n-type silicon
15 wafers having resistivities between 10 and 20 ohm-cm over a range
16 of implant energies between 250 eV and 2.2keV. Another sample
17 was implanted at a dose of $10^{15}/cm^2$ using plasma doping (PLAD)
18 (BF₃ gas). The samples were annealed using EMIH, and
19 specifically RF and microwave embodiments, to either 900 or 1000
20 degrees Celcius in an uncontrolled ambient at atmospheric
21 pressure. FIG. 6 illustrates sheet resistances versus junction
22 depth evaluated at $10^{18}/cm^3$ from SIMS. The solid line in FIG. 6
23 is the present SEMATECH barrier curve for evaluating improvements
24 in anneal and doping technology. Those of ordinary skill in the

1 art recognize that data points below the SEMATECH curve indicate
2 a higher percentage of activated dopants and/or a more efficient
3 annealed dopant profile than the SEMATECH standard.

4 Referring now to FIG. 7, there are plots of SIMS results for
5 the as-implanted and microwave spike annealed PLAD samples.
6 Those with ordinary skill in the art also recognize that a more
7 efficient profile can be obtained by a controlled ambient of
8 oxygen (e.g. 33 to 100ppm) to eliminate the oxygen-enhanced-
9 diffusion effect.

10 In one embodiment of the methods and systems disclosed
11 herein, sheet resistances were measured for implants of B+ at
12 250eV and 500eV, and BF2+ at 500eV, 1.1keV, 2.2keV, and 4.5keV,
13 with implant doses of 1.0e15/cm², using EMIH annealing, and
14 specifically, RF annealing at 13.96 MHz. In some embodiments,
15 the RF anneal time was thirty seconds to 1000 degrees Celsius and
16 900 degrees Celsius, while a spike anneal was applied in other
17 embodiments to the same temperatures. In all measured categories
18 of ion beam energy, the thirty-second, 1000 degree temperature RF
19 annealing provided the best sheet resistance, on the order of
20 nearly 300 ohms/sq. to 850 ohms/sq. The remaining experiments
21 described herein provided sheet resistances on the order of 500
22 ohms/sq to 7000 ohms/sq. Accordingly, although the RF annealing
23 activates the dopant, defects remained in the lattice structure.

1 In another embodiment where microwave EMIH annealing was
2 performed at 2.45GHz, for thirty-second and spike annealing at
3 1000 and 900 degrees Celsius, sheet resistance measurements
4 varied on the order of 150 ohms/sq. to 1000 ohms/sq. Once again,
5 defects remained in the lattice structure.

6 By performing LTRTA (i.e., approximately 500 - 800 degrees
7 Celsius) before or after EMIH annealing, defects in the lattice
8 structure caused by the implantation can be cured without the
9 undesirable diffusion effects caused by traditional RTA methods
10 that necessarily provide silicon temperatures in a range between
11 900 degrees Celsius and 1200 degrees Celsius to activate the
12 dopant. Accordingly, using the disclosed methods and systems
13 that combine EMIH with low-temperature RTA, a junction and
14 structure having high concentration dopant activation and lattice
15 repair with low diffusion and sheet resistance, can be achieved.

16 What has thus been described is a method and system to
17 achieve shallow junctions using Electromagnetic Induction Heating
18 (EMIH) that can be preceded or followed by a low-temperature
19 Rapid Thermal Annealing (RTA) process. The methods and systems
20 can use, for example, RF or microwave frequencies, to induce
21 electromagnetic fields that can induce currents to flow within
22 the silicon wafer, thus causing ohmic collisions between
23 electrons and the lattice structure that heat the wafer
24 volumetrically rather than through the surface. Such EMIH

1 heating can activate the dopant material. Defects in the silicon
2 structure can be repaired by combining the EMIH annealing with a
3 low-temperature (approximately 500 - 800 degrees Celsius) RTA
4 that causes minimal diffusion, thus minimizing the difference
5 between the as-implanted junction depth and the post-annealing
6 junction depth when compared to annealing methods that only use
7 traditional RTA.

8 The methods and systems described herein are not limited to
9 a particular hardware or software configuration, and may find
10 applicability in many computing or processing environments. The
11 methods and systems can be implemented in hardware or software,
12 or a combination of hardware and software. The methods and
13 systems can be implemented in one or more computer programs
14 executing on one or more programmable computers that include a
15 processor, a storage medium readable by the processor (including
16 volatile and non-volatile memory and/or storage elements), one or
17 more input devices, and one or more output devices.

18 Although the methods and systems have been described
19 relative to a specific embodiment thereof, they are not so
20 limited. Obviously many modifications and variations may become
21 apparent in light of the above teachings. For example, although
22 the methods and systems illustrated herein referred to silicon
23 semiconductors, other semiconductors, for example, from group IV
24 of the periodic table, can be used, as well as other

1 semiconductors. Furthermore, although the sample embodiments
2 indicated Boron (B+) as a p-type dopant, the methods and systems
3 can be applied to n-type dopants. Although LTRTA was illustrated
4 as approximately 500-800 degrees Celsius, where the LTRTA can be
5 performed using a furnace, LTRTA can be understood to include an
6 exposure to temperatures less than approximately 800 degrees
7 Celsius. The methods and systems disclosed include providing an
8 oscillating magnetic field to induce the currents in the
9 semiconductor, and although the illustrated methods and systems
10 provided RF and microwave systems, any electromagnetic wave of
11 any frequency that provides a time-varying or oscillating
12 magnetic field can be used. For example, an EMIH embodiment can
13 include a permanent magnet that can be moved to provide a time-
14 varying magnetic field.

15 Many additional changes in the details, materials, and
16 arrangement of parts, herein described and illustrated, can be
17 made by those skilled in the art. Accordingly, it will be
18 understood that the following claims are not to be limited to the
19 embodiments disclosed herein, can include practices otherwise
20 than specifically described, and are to be interpreted as broadly
21 as allowed under the law.

What is claimed is:

1. A method for annealing a semiconductor structure, the method comprising,
subjecting the semiconductor structure to an oscillating magnetic field, and,
applying a low temperature rapid thermal annealing (LTRTA) process to the semiconductor structure.
2. A method according to claim 1, wherein subjecting includes subjecting to a time-varying electromagnetic field.
3. A method according to claim 1, wherein subjecting includes providing a frequency in the microwave frequency band.
4. A method according to claim 1, wherein subjecting includes providing a frequency in the radio frequency (RF) band.
5. A method according to claim 1, wherein applying a LTRTA includes exposing the semiconductor to a temperature less than approximately 800 degrees Celsius.
6. A method according to claim 1, wherein applying a LTRTA includes exposing the semiconductor to a furnace having a

temperature greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius.

7. A method according to claim 1, wherein applying a LTRTA can precede subjecting the semiconductor to an electromagnetic field.

8. A method according to claim 1, wherein applying a LTRTA includes using a furnace to perform the LTRTA.

9. A method for implanting a dopant in a semiconductor structure, the method comprising,

 using ion implantation to implant the dopant in the semiconductor,

 activating the dopant using electromagnetic induction heating (EMIH), and,

 applying a low-temperature rapid thermal anneal (RTA) process.

10. A method according to claim 9, wherein the dopant is at least one of an n-type dopant and a p-type dopant.

11. A method according to claim 9, wherein activating the dopant using EMIH includes subjecting the dopant to an oscillating magnetic field.

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12. A method according to claim 9, wherein activating the dopant includes subjecting the dopant to a time-varying electromagnetic field.
13. A method according to claim 9, wherein activating the dopant includes providing at least one of a Radio Frequency (RF) wave and a microwave frequency.
14. A method according to claim 9, wherein applying a LTRTA includes exposing the semiconductor to a temperature less than approximately 800 degrees Celsius.
15. A method according to claim 9, wherein applying a LTRTA includes exposing the semiconductor to a furnace having a temperature greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius.
16. A method according to claim 9, wherein applying a LTRTA can precede activating the dopant.
17. A method according to claim 9, wherein applying a LTRTA includes using a furnace to perform the LTRTA.

1 Docket No. VRO-004.01

2

3 ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

4

5 ABSTRACT

6 A method and system to achieve shallow junctions using
7 Electromagnetic Induction Heating (EMIH) that can be preceded or
8 followed by a low-temperature Rapid Thermal Annealing (RTA)
9 process. The methods and systems can use, for example, RF or
10 microwave frequencies to induce electromagnetic fields that can
11 induce currents to flow within the silicon wafer, thus causing
12 ohmic collisions between electrons and the lattice structure that
13 heat the wafer volumetrically rather than through the surface.
14 Such EMIH heating can activate the dopant material. Defects in
15 the silicon structure can be repaired by combining the EMIH
16 annealing with a low-temperature (approximately 500 - 800 degrees
17 Celsius) RTA that causes minimal diffusion, thus minimizing the
18 difference between the as-implanted junction depth and the post-
19 annealing junction depth when compared to annealing methods that
20 only use traditional RTA

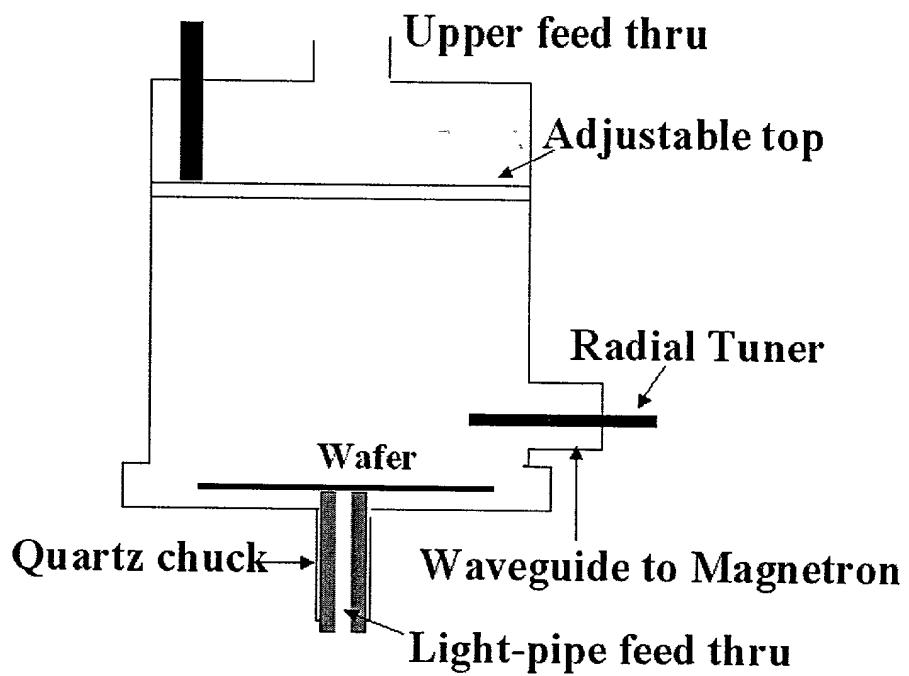
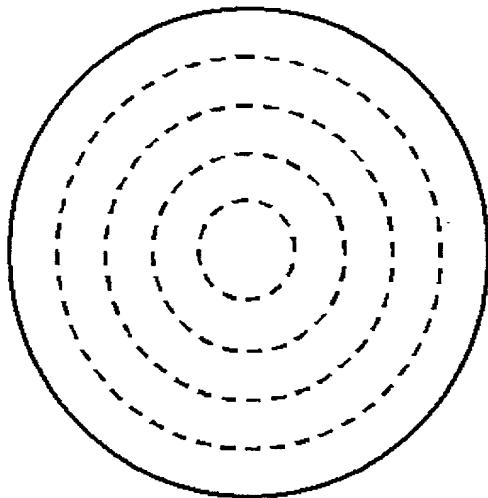


FIG. 1

TM011



TM111

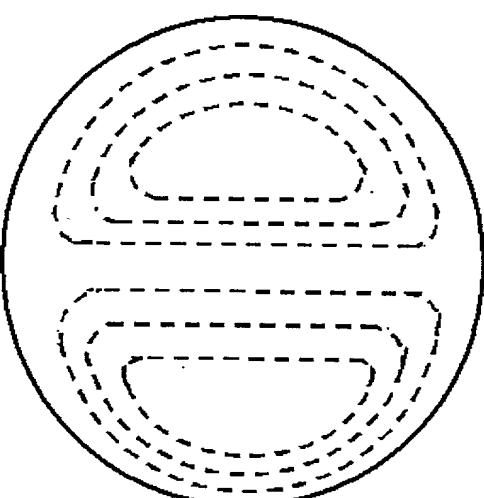


FIG. 2A

FIG. 2B

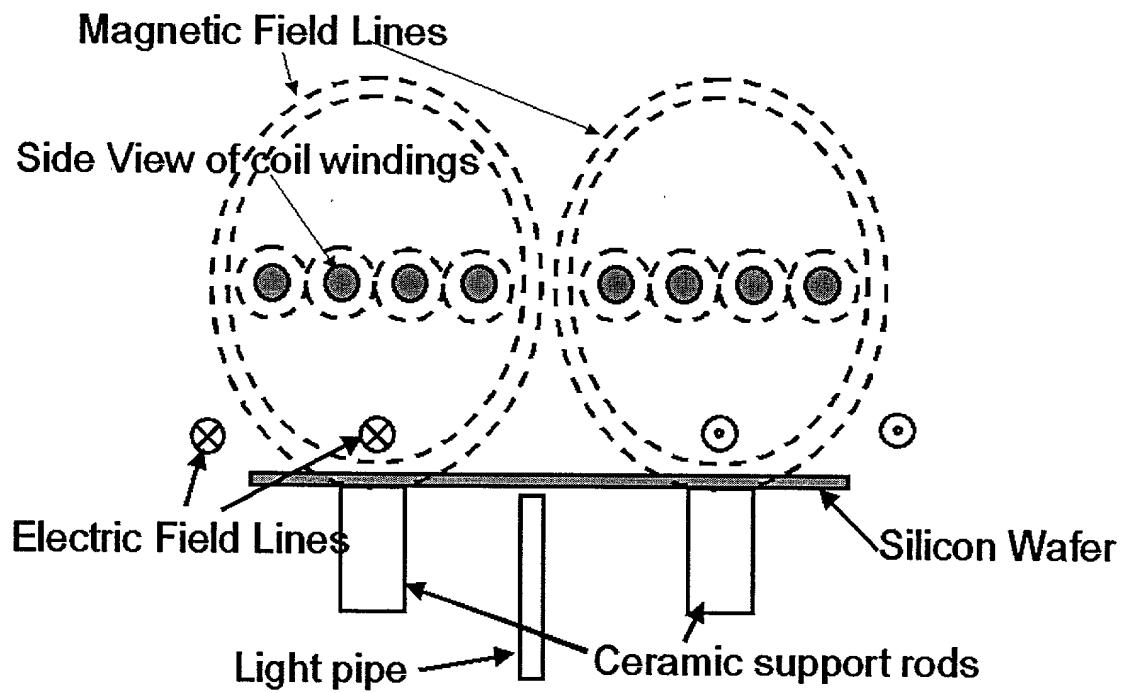


FIG. 3

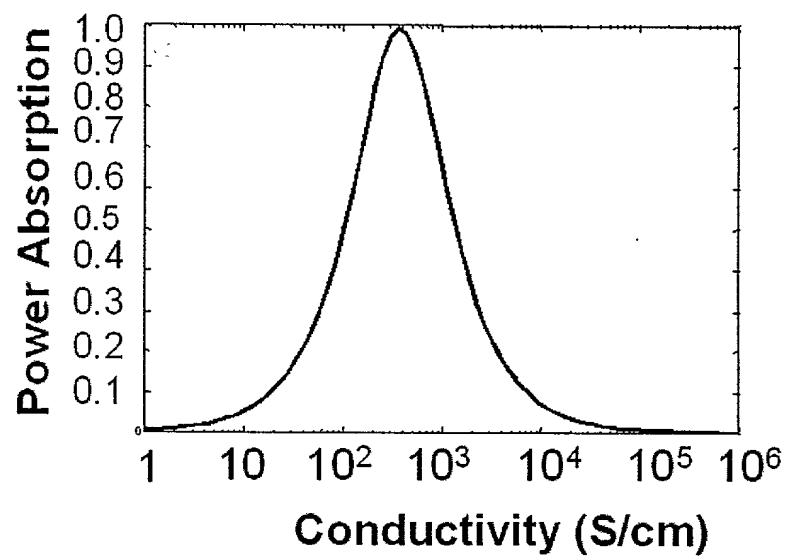


FIG. 4

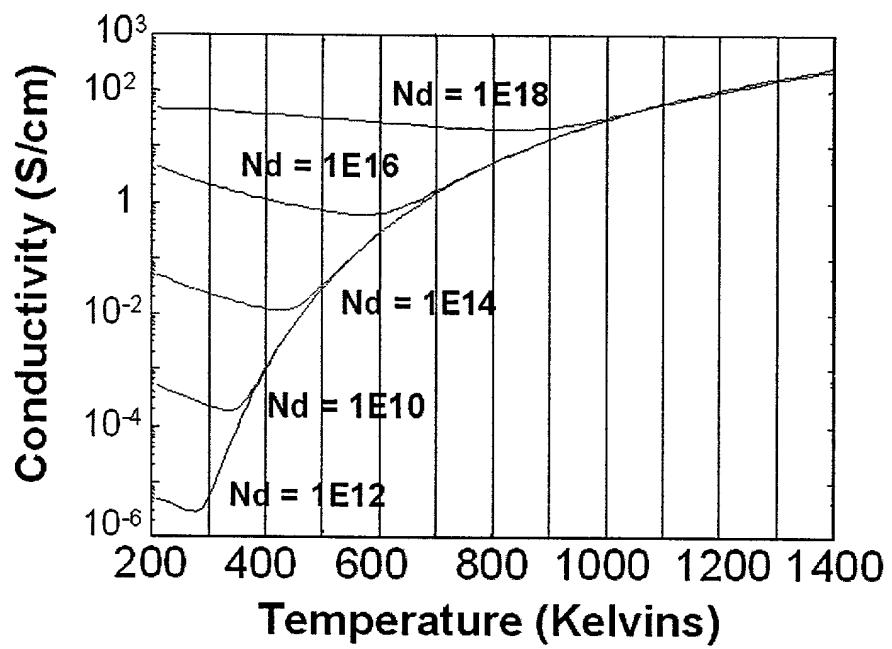


FIG. 5

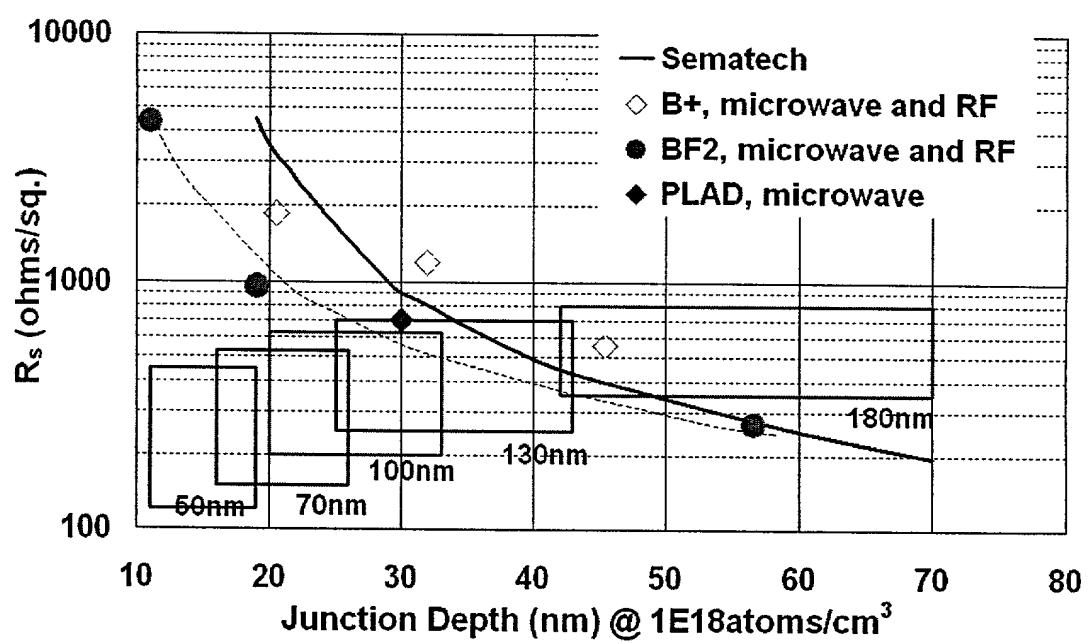


FIG. 6

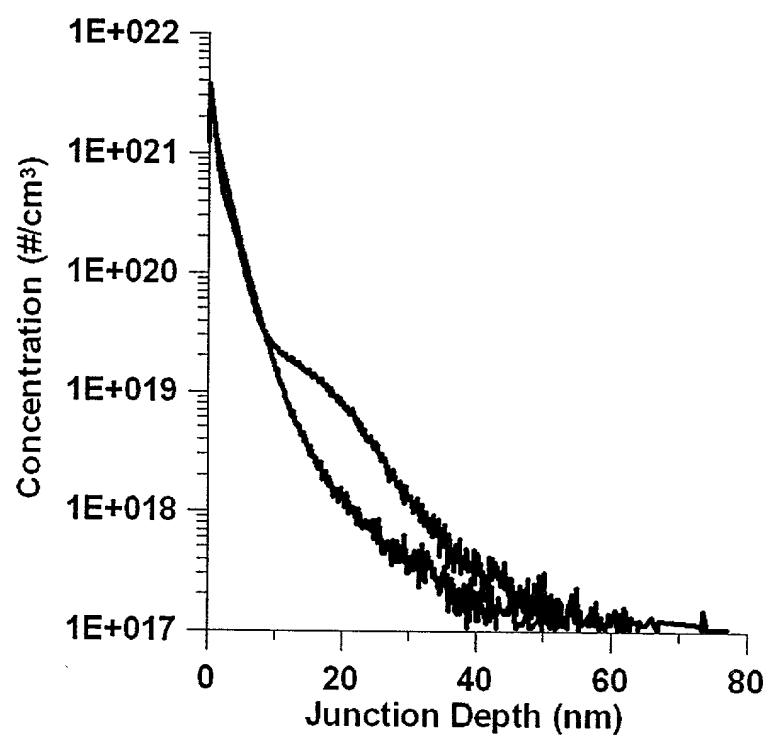


FIG. 7

DECLARATION FOR PATENT APPLICATION

Docket Number VRO-004.01

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

the specification of which (check one)

 is attached hereto. was filed on _____ as United States Application Number or PCT International Application Number _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulation, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

 Yes No (Number) (Country) (Day/Month/Year Filed) Yes No (Number) (Country) (Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States Provisional application(s) listed below.

 (Application Number) (Filing Date) (Application Number) (Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

 (Application Number) (Filing Date) (Status: patented, pending, abandoned) (Application Number) (Filing Date) (Status: patented, pending, abandoned)

I hereby appoint Beth E. Arnold, Reg. No. 35,430; Isabelle Clauss, Reg. No. 47,326; Stephen B. Deutsch, Reg. No. 46,663; William D. DeVaul Reg. No. 42,483; Daniel P. Gaudet, Reg. No. 48,584; Robert W. Gauthier, Reg. No. 35,153; Jason Gish, Reg. No. 42,581; Dana Gordon, Reg. No. 44,719; Robert A. Greenberg, Reg. No. 44,133; Jennifer K. Holmes, Reg. No. 46,778; Scott E. Kamholz, Reg. No. 48,543; David A. Lane, Reg. No. 39,261; W. Hugo Lippmann, Reg. No. 20,407; Jim Olesen, Reg. No. 46,967; Kevin A. Oliver, Reg. No. 42,049; Chinh H. Pham, Reg. No. 39,329; Jeffrey M. Sears, Reg. No. 48,440; Philip C. Swain, Reg. No. 32,376; Kingsley L. Taft, Reg. No. 43,946; John Quisel, Reg. No. 47,874; Anita Varma, Reg. No. 43,221; Sharon Webb, Reg. No. 47,172; John L. Welch, Reg. No. 28,129; and Gary L. Loser, Reg. No. 30,656 as attorneys/agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

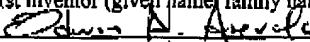
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature:		Citizenship:	Guatemalan
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